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1. **A deep-submicrometer analog-to-digital converter using focused-ion-bea**
Walden, R.H.; Schmitz, A.E.; Kramer, A.R.; Larson, L.E.; Pasiecznik, J.;
Solid-State Circuits, IEEE Journal of
Volume 25, Issue 2, April 1990 Page(s):562 - 571
Digital Object Identifier 10.1109/4.52185
AbstractPlus | Full Text: PDF(764 KB) **IEEE JNL**

2. **Compact fixed-threshold and two-vector Hamming comparators**
Pedroni, V.A.;
Electronics Letters
Volume 39, Issue 24, 27 Nov. 2003 Page(s):1705 - 1706
Digital Object Identifier 10.1049/el:20031054
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1 Detection of defective sensor elements using ΣΔ -modulation and a matched filter
D. Weiler, O. Machul, D. Hammerschmidt, B. J. Hosticka
January 2000 **Proceedings of the conference on Design, automation and test in Europe**
Full text available: pdf(88.57 KB) Additional Information: full citation, references, index terms
Publisher Site

2 Group C: energy conservation: A wake-up detector for an acoustic surveillance sensor network: algorithm and VLSI implementation
David H. Goldberg, Andreas G. Andreou, Pedro Julián, Philippe O. Pouliquen, Laurence Riddle, Rich Rosasco
April 2004 **Proceedings of the third international symposium on Information processing in sensor networks**
Full text available: pdf(483.21 KB) Additional Information: full citation, abstract, references, index terms

We describe a low-power VLSI wake-up detector for use in an acoustic surveillance sensor network. The detection criterion is based on the degree of low-frequency periodicity in the acoustic signal. To this end, we have developed a periodicity estimation algorithm that maps particularly well to a low-power VLSI implementation. The time-domain algorithm is based on the "bumpiness" of the autocorrelation of one-bit version of the signal. We discuss the relationship of this algorithm to the maximum- ...

Keywords: VLSI implementation, acoustic surveillance, maximum likelihood estimation, periodicity, power management, sensor networks, wake-up detection

3 Novel self-test methods: Ultimate low cost analog BIST
Marcelo Negreiros, Luigi Carro, Altamiro Amadeu Susin
June 2003 **Proceedings of the 40th conference on Design automation**
Full text available: pdf(207.33 KB) Additional Information: full citation, abstract, references, citings, index terms

In this work a BIST method for linear analog circuits with very low cost and the smallest possible analog overhead area is presented. The method is suitable to be implemented in the SoC environment, as it allows the reuse of resources already available in the system, and it is essentialy digital. Theoretical background is provided, and experimental results demonstrate the advantages and limits of the proposed approach.

Keywords: DSP-based analog test, low cost analog BIST, test of analog circuits

4 Innovative Applications: A dynamically reconfigurable adaptive viterbi decoder
Sriram Swaminathan, Russell Tessier, Dennis Goeckel, Wayne Burleson
February 2002 **Proceedings of the 2002 ACM/SIGDA tenth international symposium on Field-programmable gate arrays**
Full text available: pdf(235.26 KB) Additional Information: full citation, abstract, references, citings

The use of error-correcting codes has proven to be an effective way to overcome data corruption in digital communication channels. Although widely-used, the most popular communications decoding algorithm, the Viterbi algorithm, requires an exponential increase in hardware complexity to achieve greater decode accuracy. In this paper, we describe the analysis and implementation of a reduced-complexity decode approach, the adaptive Viterbi algorithm (AVA). Our AVA design is implemented in reconfigu ...

Keywords: FPGA, Viterbi coding, dynamic reconfiguration

5 Simulating sigma-delta modulators in AWEswit
Richard J. Trihy, Ronald A. Rohrer
November 1993 **Proceedings of the 1993 IEEE/ACM international conference on Computer-aided design**
Full text available: pdf(419.72 KB) Additional Information: full citation, references

6 A design strategy for low-voltage low-power continuous-time sigma-delta A/D converters
F. Gerfers, Y. Manoli
March 2001 **Proceedings of the conference on Design, automation and test in Europe**
Full text available: pdf(619.81 KB) Additional Information: full citation, references, citings, index terms

7 Low-voltage low-power switched-current circuits and systems
Nianxiong Tan, S. Eriksson
March 1995 **Proceedings of the 1995 European conference on Design and Test**
Full text available: pdf(642.50 KB) Publisher Site Additional Information: full citation, abstract, citings

This paper presents low-voltage low-power switched-current circuits and systems. Novel class AB configuration and common-mode feedforward are the essence. A delay line, memory cell, oversampling A/D converter, and chopper-stabilized oversampling A/D converter were designed and implemented. Measurement results are presented as well.

Keywords: CMOS IC, CMOS analogue integrated circuits, LV switched-current circuits, SI memory cell, analogue processing circuits, analogue storage, analogue-digital conversion, chopper-stabilized oversampling ADC, class AB configuration, common-mode feedforward, delay line, delay lines, feedforward, low-power switched-current circuits, oversampling A/D converter, sampled data circuits, switched current circuits

8 CLASS - Composite Language Approach for System Simulation (A Tutorial)
Harold G. Hixson
January 1971

Proceedings of the 5th conference on Winter simulation

Full text available: pdf(568.18 KB) Additional Information: full citation, abstract, references, index terms

There are several possible approaches to providing both discrete event and continuous system simulation capability in the same modeling context. One approach is to develop a new language which has this capability. Another, which is addressed in this tutorial, is the use of compatible languages in combination. One possibility4 involves the use of SIMSCRIPT II as the basic language. Another possibility is the use of the General Purpose Simulation System (GPSS) and its &ld ...

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L4	1517	quantize$ threshold comparators correction	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2005/07/25 10:10
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